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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,778	02/16/2005	Shigeru Umeno	ABE-026	8727

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EXAMINER	
MALEKZADEH, SEYED MASOUD	
ART UNIT	**PAPER NUMBER**
1722	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5

Office Action Summary	Application No.	Applicant(s)	
	10/524,778	UMENO ET AL.	
	Examiner	**Art Unit**	
	SEYED MASOUD MALEKZADEH	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _16 February 2005_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _20-47_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _20-47_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _16 February 2005_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _Feb 16, 2005_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23, 35, 39, and 46-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 23, 35, 39, and 46-47 claim further limitations of doped material, nitrogen and carbon, which do not further limit the scope of claims 21, 33, 37, and 42-43, respectively from which they depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al. (US 2003/0106484) in view of Wakabayashi et al (US 2006/0130737).

Fusegawa et al ('484) discloses a method for producing a silicon single crystal according to Czochralski method used for fabrication of a semiconductor device, and it also teaches while the silicon single crystal is grown, and a silicon wafer with significantly high quality can be produced in high productivity by controlling a concentration of interstitial oxygen in a silicon single crystal to be low [See paragraph (0001)]. Moreover, it discloses if a silicon wafer manufactured from a silicon single crystal having high interstitial oxygen concentration is subjected to heat treatment, for example, at high temperature of 1150°C in an oxidizing atmosphere for about 2 hrs [See paragraph 13]. Furthermore, it discloses the concentration of interstitial oxygen in a silicon single crystal wafer is 6×10^{17} to 10×10^{17} atoms $/cm^3$ [See paragraph (0030)] which concentration of interstitial oxygen was measured by FT-IR (Fourier Transform Infrared Spectroscopy) [See paragraph 85]. It also teaches the silicon ingot can be processed into a wafer of the present invention by subjecting it to slicing and

mirror-finish-polishing [See paragraph (0074)]. However, it does not teach the relationship between interstitial oxygen concentration and heat treatment temperature.

In the analogous art, Wakabayashi et al. teaches a method for manufacturing a silicon single crystal whose diameter is suppressed from being fluctuated by subjecting a silicon single crystal rod pulled up by a Czochralski method to a PID control [See paragraph (0001)]. Further it teaches the ratios between the concentration of vacancies and interstitial oxygen and temperature are as follows, respectively:

$$C_v^e = K_1 \exp(-E_v / kT)$$

$$C_i^e = K_2 \exp(-E_i / kT)$$

Where C_v is the concentration of the vacancies and C_i is the concentration of interstitial silicon, K_1 and K_2 are constants, Ei and E_v are formation energies of interstitial silicon and the vacancies, k is a Boltzman constant, and T is an absolute temperature [See paragraph (0082) and (0083)] which absolute temperature for 0 K is equal to –273.15 °C. The relationship between concentration of interstitial oxygen and heat treatment temperature can follow the similar relationship between concentration of vacancies and concentration of interstitial silicon with temperature as discussed above.

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to increase confidence level in overall process control and product capability for a silicon wafer of Fusegawa et al. ('484) to consider the

relationship between interstitial oxygen concentration [Oi] and temperature in order to know the strength of silicon wafer since oxygen is effective for enhancing the strength of a silicon wafer as suggested by Wakabayashi et al ('737).

Claims 21, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484) and Wakabayashi et al ('737) and further in view of Haas et al (US 4,119,441) and Kobayashi (US2006/0024915).

Fusegawa et al ('484) and Wakabayashi et al ('737) disclose the limitations of a manufacturing method of a silicon single crystal wafer. Moreover, Fusegawa et al ('484) also teaches the silicon ingot can be processed into a wafer by subjecting it to slicing and mirror-finish-polishing [See paragraph (0074)] as discussed above but do not teach that single crystal used to manufacture of silicon wafer is doped with phosphorus by a neutron irradiation and further do not teach a manufacturing method for SOI wafer.

In the analogous art, Haas et al ('441) discloses a method for the production of n-doped silicon single crystals that this silicon single crystal is exposed to a pattern of radiation. The neutron radiation causes a weaker doping concentration in marginal regions of the crystal due to the production of fewer phosphorus atoms [See abstract]. Further, Kobayashi ('915) discloses a method of manufacturing an SOI wafer comprising the steps of forming an insulating layer on at least one wafer of two starting wafers and adhering the one wafer to the other wafer without an adhesive [See paragraph (0097)].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope silicon wafer manufactured by method of Fusegawa

et al ('484) and Wakabayashi et al ('737) with phosphorus by using a neutron irradiation in order to decrease crystal damage and making a specific resistance in the silicon single crystal as suggested by Haas et al ('441), and manufacturing a SOI wafer as suggested by Kobayashi ('915) in order to use high resistivity of SOI wafer to reduce signal transmission loss which is especially useful with high frequency devices.

Claims 22, 26, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484) and Wakabayashi et al ('737) and further in view of Asayama et al (US 6,641,888) and Kobayashi ('915).

Fusegawa et al ('484) and Wakabayashi et al ('737) disclose the limitations of a manufacturing method of a silicon single crystal wafer, and moreover, Fusegawa et al ('484) also teaches the silicon ingot can be processed into a wafer by subjecting it to slicing and mirror-finish-polishing [See paragraph (0074)] as discussed above but does not teach that single crystal used to manufacture of silicon wafer is doped with nitrogen by a concentration of $2\times10^{13}\ atoms/cm^3$ or more and/or with carbon by a concentration of $5\times10^{16}\ atoms/cm^3$ or more and further do not teach the manufacturing method of SOI wafer.

In the analogous art, Asayama et al. ('888) present an invention which relates to a silicon single crystal used for a semiconductor integrated circuit device and to a silicon wafer and an epitaxial wafer [See lines 9-15, column 1]. Further, Asayama et al. ('888) discloses the silicon single crystal is grown with nitrogen doping at a concentration of $1\times10^{13}\ atoms/cm^3$ or more, or with nitrogen

doping at a concentration of 1×10^{12} $atoms/cm^3$ and carbon doping at a concentration of 0.1×10^{16} - 5×10^{16} $atoms/cm^3$ [See abstract]. Further Kobayashi ('915) discloses a method of manufacturing an SOI wafer comprising the steps of forming an insulating layer on at least one wafer of two starting wafers and adhering the one wafer to the other wafer without an adhesive [See paragraph (0097)].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope silicon wafer manufactured by method of Fusegawa et al ('484) and Wakabayashi et al ('737) with nitrogen and carbon in order to control the resistance of the silicon single crystal as suggested by Asayama et al. ('441), and manufacturing a SOI wafer as suggested by Kobayashi ('915) in order to use high resistivity of SOI wafer to reduce signal transmission loss which is especially useful with high frequency devices.

Claims 23, 27, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), Wakabayashi et al ('737), Haas et al ('441), and further in view of Asayama et al. ('888), and Kobayashi et al ('915).

Fusegawa et al ('484), Wakabayashi et al ('737), and Hass et al ('441) disclose the limitations of a manufacturing method of a silicon single crystal wafer and moreover, Fusegawa et al ('484) also teaches the silicon ingot can be processed into a wafer by subjecting it to slicing and mirror-finish-polishing [See paragraph (0074)] as discussed above but does not teach that single crystal used to manufacture of silicon wafer is doped with nitrogen by a concentration of 2×10^{13} $atoms/cm^3$ or more and/or with carbon by a concentration of

5×10^{16} $atoms/cm^3$ or more, and further do not teach the manufacturing method of SOI wafer.

In the analogous art, Asayama et al. ('888) present an invention which relates to a silicon single crystal used for a semiconductor integrated circuit device and to a silicon wafer and an epitaxial wafer [See lines 9-15, column 1]. Further, Asayama et al. ('888) discloses the silicon single crystal is grown with nitrogen doping at a concentration of 1×10^{13} $atoms/cm^3$ or more, or with nitrogen doping at a concentration of 1×10^{12} $atoms/cm^3$ and carbon doping at a concentration of 0.1×10^{16} - 5×10^{16} $atoms/cm^3$ [See abstract]. Further Kobayashi ('915) discloses a method of manufacturing an SOI wafer comprising the steps of forming an insulating layer on at least one wafer of two starting wafers and adhering the one wafer to the other wafer without an adhesive [See paragraph (0097)].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope silicon wafer manufactured by method of Fusegawa et al ('484), Wakabayashi et al ('737), and Haas et al. ('441) with nitrogen and carbon in order to control the resistance of the silicon single crystal as suggested by Asayama et al. ('441), and manufacturing a SOI wafer as suggested by Kobayashi ('915) in order to use high resistivity of SOI wafer to reduce signal transmission loss which is especially useful with high frequency devices.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), Wakabayashi et al ('737) and further in view of Kobayashi (US 2006/0024915)

Fusegawa et al ('484) and Wakabayashi et al ('737) disclose the limitations of a manufacturing method of a silicon single crystal wafer, and moreover, Fusegawa et al ('484) also teaches the silicon ingot can be processed into a wafer by subjecting it to slicing and mirror-finish-polishing [See paragraph (0074)] as discussed above but do not teach the manufacturing method of SOI wafer.

In the analogous art, Kobayashi ('915) Kobayashi ('915) discloses a method of manufacturing an SOI wafer comprising the steps of forming an insulating layer on at least one wafer of two starting wafers and adhering the one wafer to the other wafer without an adhesive [See paragraph (0097)]

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to use silicon wafer manufactured by method of Fusegawa et al ('484), Wakabayashi et al ('737) for manufacturing a SOI wafer as suggested by Kobayashi ('915) in order to using high resistivity of SOI wafer to reduce signal transmission loss, which is especially useful with high frequency devices.

Claims <u>32, 36, 40, and 41</u> are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), Wakabayashi et al ('737) and further in view of Sakurada et al. (US 2005/006432).

Fusegawa et al ('484) and Wakabayashi et al ('737) disclose the limitations of a manufacturing method of a silicon single crystal wafer as discussed in claim 1 but do not teach the manufacturing method of SOI wafer.

In the analogous art, Sakurada et al ('032) teaches a method of producing an SOI wafer, which through a bonding method two silicon wafers are bonded together via an oxide film. In ion implantation delemination method which is one of bonding methods, an oxide film (an insulator layer) is formed on a surface of a silicon wafer (a bond wafer) to be a silicon active layer or a base wafer to be a support substrate, and an ion implanted layer is formed inside the bond wafer by implanting ions such as hydrogen from one side surface of the bond wafer. Further, after this bond wafer is bonded to the base wafer via the oxide film, delemination is performed at the ion-implanted layer by heat treatment. Thereby, an SOI wafer in which a thin silicon active layer is formed on the base wafer via the oxide film can be obtained [See paragraph (0002)]. It further disclose when performing oxidation treatment for bonding the bond wafer and the base wafer together and oxidation treatment for adjusting the thickness of an SOI layer, and subsequently cleaning with hydrofluoric acid to remove an oxide film, even if the silicon single crystal grown is used as the bond wafer, there has been the case that a failure such that the SOI layer was almost entirely or partially destroyed could occurred [See paragraph (0016)]. Moreover, it teaches in the process bonding heat treatment, the SOI wafer is subjected to a bonding heat treatment. In this process, since bonding strength between the wafers brought into close contact in the bonding step and the delamination heat treatment step is too weak to be used as it is in a device fabrication process, the SOI wafer is subjected to a heat treatment to be sufficient bonding strength [See paragraph (0072)]. It also discloses which the wafers are separated into a delaminated wafer and an SOI

wafer which this SOI wafer can contain an SOI layer, a buried oxide film, and a base wafer [See paragraph (0071)]. It further teaches that after pulling the crystal, wafers were cut out in order from the head side of each crystal block in the direction of the crystal growth axis then the wafers were cutting and the wafers were mirror-polished [See paragraph (0097)]. It also discloses the steps of producing SOI wafer are as follows: formation of oxide film, ion Implantation, bonding delamination heat treatment, removal of oxide film, oxidation for adjusting SOI layer, and removal of oxide film [See Figure 1].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to use silicon wafer manufactured by method of Fusegawa et al ('484), Wakabayashi et al ('737) for manufacturing a SOI wafer as suggested by Sakurada et al ('632) in order to use high resistivity of SOI wafer to reduce signal transmission loss, which is especially useful with high frequency devices.

Claims 33, 37, and 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484) and Wakabayashi et al ('737), Sakurada et al ('632) and further in view of Haas et al (US 4,119,441)

Fusegawa et al ('484) and Wakabayashi et al ('737), Sakurada et al ('632) disclose the limitations of a manufacturing method of a SOI wafer from a silicon single crystal wafer as discussed above but do not teach that single crystal used to manufacture of SOI wafer is doped with phosphorus by a neutron irradiation.

In the analogous art, Haas et al ('441) discloses a method for the production of n-doped silicon single crystals that this silicon single crystal is

exposed to a pattern of radiation. The neutron radiation causes a weaker doping concentration in marginal regions of the crystal due to the production of fewer phosphorus atoms [See abstract].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope active layer side of silicon wafer used to manufacture SOI wafer by method of Fusegawa et al ('484) and Wakabayashi et al ('737), Sakurada et al ('632) with phosphorus by using a neutron irradiation in order to decrease crystal damage and making a specific resistance in the silicon single crystal as suggested by Haas et al ('441).

Claims 34, 38, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), Wakabayashi et al ('737), Sakurada et al ('632), and further in view of Asayama et al (US 6,641,888).

Fusegawa et al ('484), Wakabayashi et al ('737), and Sakurada et al ('632) disclose the limitations of a manufacturing method of a SOI wafer from a silicon single crystal wafer as discussed above but do not teach that single crystal used to manufacture of SOI wafer is doped with nitrogen by a concentration of 2×10^{13} $atoms/cm^3$ or more and/or with carbon by a concentration of 5×10^{16} $atoms/cm^3$ or more.

In the analogous art, Asayama et al. ('888) present an invention which relates to a silicon single crystal used for a semiconductor integrated circuit device and to a silicon wafer and an epitaxial wafer [See lines 9-15, column 1]. Further, Asayama et al. ('888) discloses the silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13}

$atoms/cm^3$ or more, or with nitrogen doping at a concentration of 1×10^{12} $atoms/cm^3$ and carbon doping at a concentration of 0.1×10^{16} - 5×10^{16} $atoms/cm^3$ [See abstract].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope active layer side of silicon wafer used to manufacture SOI wafer by method of Fusegawa et al ('484) and Wakabayashi et al ('737), Sakurada et al ('632) with nitrogen and carbon in order to control the resistance of the silicon single crystal as suggested by Asayama et al. ('441)

Claims 35, 39, 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusegawa et al ('484), Wakabayashi et al ('737), Sakurada et al ('632), Haas et al ('441), and further in view of Asayama et al. ('888).

Fusegawa et al ('484), Wakabayashi et al ('737), and Sakurada et al ('632), Haas et al ('441) disclose the limitations of a manufacturing method of a SOI wafer from a silicon single crystal wafer as discussed above but do not teach that single crystal used to manufacture of SOI wafer is doped with nitrogen by a concentration of 2×10^{13} $atoms/cm^3$ or more and/or with carbon by a concentration of 5×10^{16} $atoms/cm^3$ or more.

In the analogous art, Asayama et al. ('888) present an invention which relates to a silicon single crystal used for a semiconductor integrated circuit device and to a silicon wafer and an epitaxial wafer [See lines 9-15, column 1]. Further, Asayama et al. ('888) discloses the silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13}

$atoms/cm^3$ or more, or with nitrogen doping at a concentration of 1×10^{12} $atoms/cm^3$ and carbon doping at a concentration of 0.1×10^{16} - 5×10^{16} $atoms/cm^3$ [See abstract].

It would have been obvious to one of ordinary skill in this art at the time of applicant's invention to dope silicon wafer manufactured by method of Fusegawa et al ('484), Wakabayashi et al ('737), Sakurada et al ('632), and Haas et al. ('441) with nitrogen and carbon in order to control the resistance of the silicon single crystal as suggested by Asayama et al. ('441)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seyed Masoud Malekzadeh whose telephone number is 571-272-6215. The examiner can normally be reached on Monday – Friday at

8:30 am – 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra N. Gupta can be reached on (571) 272-1316. The fax number for the organization where this application or proceeding is assigned is

571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance form a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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